

## Description

# NONVOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING DIVIDED BIT LINES

### CROSS REFERENCE TO RELATED APPLICATIONS

[0001] In this divisional application, the specification and drawings are carried forward from the application Ser. No. 09/956,212, filed 09/18/2001 without any amendment.

### BACKGROUND OF INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor memory device. More specifically, the present invention relates to a Nonvolatile semiconductor memory device having divided bit lines.

[0004] 2. Description of the Prior Art

[0005] In a non-volatile memory, a flash memory can be programmed by channel hot electron injection, also known as Fowler-Nordheim tunneling. In programming, electrons

are driven into a floating gate to increase a critical voltage of a memory cell. In erasing, the electrons are drawn from the floating gate to decrease the critical voltage of the memory cell.

[0006] Figs. 1A shows a configuration of bit lines of a conventional flash memory. Fig. 1B shows circuit schematic drawing of a conventional flash memory. The conventional flash memory has an N-type substrate 10, a deep P-well 12 and an N-well 14. A plurality of memory cells is formed inside the N-well 14. For example, a memory cell 16 includes a drain 18, a gate 20 and a source 22. The drain 18 and the source 22 are formed of N-type ion regions. The gate consists of a control gate 24 that connects to a gate voltage and a floating gate 26 located under the control gate 24. The source 22 is surrounded by a P-type ion region 28. The bit line 30 penetrates a source shown as a reference numeral 22 and a P-type ion region shown as a reference numeral 28.

[0007] All the above memory cells are formed on the same N-well 14. When a programming process is performed, the power from the bit line affects the memory cells connected to the same bit line but not selected. For example, when 5V are applied to the bit line (source) and 0V to the

word line (gate), slightly less than 5V exist on the drain of the non-selected memory cells. This forms  $M-1$  disturbances in the selected sector and  $M * P/E$  (program/erase) cycle times  $*(N-1)$  if the device has  $N$  sectors each of which has  $M$  word lines, wherein  $M$  is equal to the number of the memory cells. Therefore, the total disturbances during programming the bit line is  $M * P/E$  cycle times  $*(N-1)+(M-1)$ .

[0008] Performance of an erasing process also generates disturbances. The sectors are erased wholly, not respectively. When 8V are applied to the drain, the voltage for the whole N-well is maintained at about 8V. Therefore,  $P/E$  cycle times  $*(N-1)$  of disturbances are generated in other sectors during erasing the bit line.

[0009] The disturbances generated during programming or erasing the bit line affect data storage of the memory cell. Furthermore, connection between a source and P-type ion region in each memory cell by the bit line forms a parasitic capacitance 32 at the source, as shown in Fig. 1B. In a reading process, the capacitance burdens the bit line and thus lowers the reading speed.

## **SUMMARY OF INVENTION**

[0010] It is one object of the present invention to provide a non-

volatile semiconductor memory device having divided bit lines to prevent the above overloading of the bit lines from being generated.

[0011] It is another object of the present invention to provide a non-volatile semiconductor memory device having divided bit lines to effectively reduce disturbances when programming or erasing bit lines.

[0012] To achieve the above and other objects of the present invention, a non-volatile semiconductor memory device having divided bit lines is provided. The memory device includes a substrate, a plurality of memory cells, at least one bit line selection device, at least one isolation structure, a main bit line and at least one sub bit line.

[0013] The substrate has an N-type region, a deep P-well and an N-well from the bottom to the top. The memory cells are located inside the N-well, with a designated number of the memory cells form a sector. The bit line selection device is located inside the N-well and between sectors to control operation of any sector. An isolation structure is located between the sector of the memory cells and the bit line selection device. The main bit line is electrically connected to one end of the bit line selection device. The sub bit line is electrically connects all memory cells in

each sector to the other end of the bit line selection device, respectively.

[0014] Since the sub bit line is controlled by the bit line selection device, the bit line voltage for the memory cells in the non-selected sector is in the floating state, such that the memory cells in the non-selected sector are in a non-operational state and no parasitic capacitance is generated. Thereby, overloading of the bit line can be avoided.

[0015] Each of the above memory cells has a source, a gate and a drain. The source consists of an N-type ion region surrounded by a P-type ion region. A short circuit connection between the source and the P-type ion region is formed. The short circuit connection can be also formed by a metal layer penetrating the source and the P-type ion region. Alternatively, the short circuit connection can be formed by a metal layer connecting an exposed source to the P-type ion region. The drain consists of an N-type ion region and connects to the P-type ion region. Alternatively, the drain comprises an N<sup>+</sup> ion region and an N<sup>-</sup> ion region that is located between the N<sup>+</sup> ion region and the P-type ion region. In one embodiment, the drain comprises an N<sup>+</sup> ion region and an N<sup>-</sup> ion region than surrounds the N<sup>+</sup> ion region and connects to the P-type ion

region. In another embodiment, the drain region comprises an N<sup>+</sup> ion region and an N-type field oxide located between the N<sup>+</sup> ion region and the P-type ion region.

[0016] The sub bit line and the main bit line can be made of metal or a metallic compound. Every sixteen or more of the memory cells form a sector. Each memory cell has a gate, a source and a drain. A word line voltage, a bit line voltage and a drain voltage are applied to the gate, the bit line and the drain, respectively. When an erasing process is performed, a high level of word line voltage and a drain voltage relatively lower than the word line voltage are provided, keeping the bit line voltage in a suspended state and a deep P-well at a voltage relatively lower than the word line voltage. When a programming process is performed, a low level of word line voltage and the bit line voltage relatively higher than the word line voltage are provided, keeping the drain in the suspended state and the deep P-well at a voltage relatively higher than the word line voltage. When a reading process is performed, a higher level of the word line voltage, a drain voltage relatively lower than the word line voltage, a bit line voltage relatively lower the drain voltage, and a deep P-well voltage relatively lower than the drain voltage are provided.

[0017] In a second aspect of the present invention, a non-volatile semiconductor memory device having divided bit lines is provided. The memory device includes a substrate, a plurality of memory cells, at least one bit line selection device, at least one isolation structure, a main bit line and at least one bit line.

[0018] The substrate includes an N-type region, a deep P-well and a combined well from the bottom to the top. The combined well consists of a P-well and an N-well in parallel. The memory cells are located inside the N-well, wherein a designated number of the memory cells form a sector. The bit line selection device is located inside the P-well and between sectors to control operation of any sector. An isolation structure is located between the P-well and the N-well to isolate the sector of the memory cells from the bit line selection device. The main bit line is electrically connected to one end of the bit line selection device. The sub bit line electrically connects all memory cells in each sector to the other end of the bit line selection device, respectively.

[0019] The P-well and the N-well are arranged in parallel in the combined well. The bit line selection device is located in the P-well and the memory cells are in the N-well, such

that it is not necessary to share the same N-well and thus reduced disturbances generated during programming or erasing the bit lines can be achieved.

[0020] Each of the above memory cells has a source, a gate and a drain. The source consists of an N-type ion region surrounded by a P-type ion region. A short circuit connection between the source and the P-type ion region is formed. The short circuit connection can be also formed by a metal layer penetrating the source and the P-type ion region. Alternatively, the short circuit connection can be formed by a metal layer connecting an exposed source to the P-type ion region. The drain consists of an N-type ion region and connects to the P-type ion region. Alternatively, the drain comprises an N<sup>+</sup> ion region and an N<sup>-</sup> ion region that is located between the N<sup>+</sup> ion region and the P-type ion region. In one embodiment, the drain comprises an N<sup>+</sup> ion region and an N<sup>-</sup> ion region than surrounds the N<sup>+</sup> ion region and connects to the P-type ion region. In another embodiment, the drain region comprises an N<sup>+</sup> ion region and an N-type field oxide that located between the N<sup>+</sup> ion region and the P-type ion region.

[0021] The sub bit line and the main bit line can be made of



metal or a metallic compound. Every 16 or more of the memory cells form a sector. Each memory cell has a gate, a source and a drain. A word line voltage, a bit line voltage and a drain voltage are applied to the gate, the bit line and the drain, respectively. When an erasing process is performed, a high level of word line voltage and a drain voltage relatively lower than the word line voltage are provided, keeping the bit line voltage in a suspended state and a deep P-well at a voltage relatively lower than the word line voltage. When a programming process is performed, a low level of word line voltage is applied and the bit line voltage is relatively higher than the word line voltage, keeping the drain in the suspended state and the deep P-well at a voltage relatively higher than the word line voltage. When a reading process is performed, a higher level of the word line voltage, a drain voltage relatively lower than the word line voltage, a bit line voltage relatively lower than the drain voltage, and a deep P-well voltage relatively lower than the drain voltage are provided.

#### **BRIEF DESCRIPTION OF DRAWINGS**

[0022] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of

the invention as claimed.

[0023] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principle of the invention. In the drawings,

[0024] Figs. 1A shows a configuration of bit lines of a conventional flash memory;

[0025] Fig. 1B shows circuit layout of a conventional flash memory;

[0026] Figs. 2A and 2B show a non-volatile semiconductor memory device having divided bit lines according to one preferred embodiment of the present invention;

[0027] Figs. 3A and 3B show a non-volatile semiconductor memory device having divided bit lines according another preferred embodiment of the present invention;

[0028] Fig. 4A shows locally enlarged view of the memory device of Fig. 3A;

[0029] Fig. 4B shows another type of the memory cell;

[0030] Fig. 4C shows still another type of the memory cell;

[0031] Fig. 4D shows further another type of the memory cell;

- [0032] Fig. 5A is an enlarged view showing a sub bit line 112 connected to a memory cell in Fig. 3A;
- [0033] Fig. 5B shows another connection for the bit lines; and
- [0034] Figs. 6A–6C show programming, erasing and reading of a non-volatile semiconductor memory device having divided bit lines according to the present invention.

#### **DETAILED DESCRIPTION**

- [0035] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Whenever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.
- [0036] Figs. 2A and 2B show a non-volatile semiconductor memory device having divided bit lines according to one preferred embodiment of the present invention.
- [0037] The non-volatile semiconductor memory device of this embodiment of the present invention includes a substrate 50, a plurality of memory cells (such as 52 and 54), at least a bit line selection device 56 such as a P channel MOS transistor, at least an isolation structure 68 such as an isolation made of oxide, a main bit line 58 and at least

a sub bit line 60.

[0038] The substrate 50 has an N-type region 62, a deep P-well 64 and an N-well 66. Memory cells 52 and 54 are located inside the N-well 66. A sector of memory cells can consist of 16, 32, 64 or more than 64 memory cells. As shown in Figures, the memory cells 52 and 54 form a sector 70 and memory cells 74 and 76 form a sector 72. The bit line selection device 56 such as a P channel MOS transistor is located inside the N-well 66 and between each sector of the memory cells to control all sectors of the memory cells. The isolation structure 68 is located between the memory cell 52 and the bit line selection device 56. The bit line has one end 78, which is a P-type region and another end 80, which is also a P-type region. The main bit line 58 is electrically connected to one end 78 of the bit line selection device 56. The sub bit line 60 is electrically connected to each sector of the memory cells, such as a source 84 of the memory cell 52 in the sector 70, to the end 80 of the bit line selection device 56. The above main bit line and the sub bit line can be made of metal or a metallic compound.

[0039] With reference to Fig. 2A, no voltage is applied to the main bit line 58. If the memory cell 52 is read, then the bit

line selection device 56 is connected and the other control bit line selection device 82 is disconnected, such that the sub bit line 60 and the main bit line 58 have the same voltages and the sub bit line 86 is in a suspended state. The memory cells that are designated to not be operated do not generate any parasitic capacitance and bit line loading, so that the loading of the main bit line can be reduced when the reading process is performed.

[0040] The above configuration performs programming by using the same N-well. However, when 5V are applied to the main bit line 58, about 5V are formed on the N-well. This forms  $M-1$  disturbances in the selected sector and  $M \times P/E$  (program/erase) cycle times  $\times (N-1)$  if the device has  $N$  sectors each of which has  $M$  word lines,  $M$  being equal to the number of the memory cells. Therefore, the total disturbances during programming the bit line is  $M \times P/E$  cycle times  $\times (N-1) + (M-1)$ .

[0041] Also, when the erasing process is performed, disturbances of the bit line are erased wholly, not respectively. Disturbances of the bit line are erased  $P/E$  cycle times  $\times (N-1)$  in other sectors.

[0042] Figs. 3A and 3B show a non-volatile semiconductor memory device having divided bit lines according another pre-

ferred embodiment of the present invention, which can provide reduced disturbance when reading and erasing the bit line.

[0043] The non-volatile semiconductor memory device of this embodiment of the present invention includes a substrate 100, a plurality of memory cells 102 and 104, a bit line selection device 106, an isolation structure 108, a main bit line 110 and a sub bit line 112.

[0044] The substrate 100, different from the substrate 50 shown in Fig. 2A, has an N-type region 114, a deep P-well 116 and a combined well region 118. The combined well region 118, different from the single N-well 14 shown in Fig. 2A, consists of a P-well 120 and an N-well 122 in parallel. The memory cells 102 and 104 are arranged inside the N-well 122. Sixteen or more memory cells form a sector. Additionally, one or more sectors are formed on the same N-well. For example, two adjacent sectors are formed on the same N-well. The bit line selection device 106 such as N channel MOS transistor is provided in the P-well 120, which is different from Fig. 2A, and located between sectors to control the operation of any sector. The isolation structure 108 is located between the P-well 120 and the N-well 122 to isolate a sector, such as a sec-

tor 124 of memory cells 102 and 104, from the bit line selection device 106. The main bit line 110 is electrically connected to one end 126 of the bit line selection device 106. The sub bit line 112 is electrically connected to a source of the memory cell in the sector 124 and to the other end 128 of the bit line selection device 106.

[0045] Further, the P-well 120 also provides isolation between N-wells 122 and 130, such that each sector of memory cells are in different N-wells and isolated by the P-well. Therefore, the disturbances caused by reading and erasing the bit line using the same N-well in the conventional process can be prevented. Only M-1 programming bit line disturbances are generated in the same N-well during a programming process. The disturbances generated in the present memory device are greatly reduced compared to the conventional one.

[0046] The memory cell indicated by reference numeral 52 in Fig. 2A or 102 in Fig. 3A is not limited to the above specified embodiments. The memory cell 102 located in the N-well has a source 200, a gate region 202 and a drain 204 as shown in Fig.4A. The gate 202 includes a control gate 206 and a floating gate 208 thereunder. The source 200 consists of an N-type ion region surrounding by a P-type ion

region 210. The drain 204 consists of an N-type region adjacent to the P-ion-type region 210.

[0047] Fig. 4B shows another type of the memory cell. The memory device shown in Fig. 4B has the same gate and source as those shown in Fig. 4A. The drain in this embodiment includes an N- ion region 220 and an N+ ion region 222. The N- ion region 220 is located between the N+ ion region 222 and the P-type ion region 224.

[0048] Fig. 4C shows still another type of the memory cell. The memory cell shown in Fig. 4C has the same gate and source as those shown in Fig. 4A. The drain in this embodiment includes an N- ion region 230 and an N+ ion region 232. However, Fig. 4C differs from Fig. 4B in that the N- ion region 230 surrounds the N+ ion region 232 and connects to the P-type ion region 234.

[0049] Fig. 4D shows yet another type of the memory cell. The memory cell shown in Fig. 4C has the same gate and source as those shown in Fig. 4A. The drain in this embodiment includes an N-type field oxide 240 and an N+ ion region 242. The N-type field oxide 240 is located between N+ ion region 242 and a P-type ion region 244.

[0050] Fig. 5A is an enlarged view showing a sub bit line 112 that is connected to a memory cell in Fig. 3A. A short circuit



connects a source 300 and a P-type ion region 302. For example, a metal layer 304 connected to the bit line 112 penetrates the source 300 and the P-type ion region 302, as shown in Fig. 5A. Alternatively, a metal layer 306 connects the exposed source 308 to the P-type ion region 310 to form a short circuit connection as shown in the Fig.5B.

[0051] Figs. 6A–6C show programming, erasing and reading of a non-volatile semiconductor memory device having divided bit lines according to the present invention. In Fig. 6A, a word line voltage  $V_{WL}$ , a bit line voltage  $V_{BL}$  and a drain voltage  $V_{DL}$  are applied to a gate 400, a source 402 and a drain 404, respectively.

[0052] When the erasing process is performed, as shown in Fig. 6A, a high level of word line voltage  $V_{WL}$  such as 8V~ 12V and a drain voltage  $V_{DL}$  relatively lower than the word line voltage  $V_{WL}$  such as -12V~ -8V are provided, keeping the bit line voltage  $V_{BL}$  in a suspended state and a deep P-well 406 at the same voltage as the drain such as -12V~ -8V. Under the operation recited above, electrons move into a floating gate 408.

[0053] When a programming process is performed as shown in Fig. 6B, a low level of word line voltage  $V_{WL}$  such as -12V~

-8V and the bit line voltage  $V_{BL}$  relatively higher than the word line voltage  $V_{WL}$  such as 3V – 7V are provided, keeping the drain in the suspended state and the deep P-well 406 at a voltage relatively higher than the word line voltage  $V_{WL}$  and lower than the bit line voltage  $V_{BL}$ , such as 0V. Under the operation recited above, electrons move into the source 402 and the P-type ion region 410 from the floating gate 408.

[0054] When a reading process is performed as shown in Fig. 6C, a higher level of the word line voltage  $V_{WL}$  such as 2V – 5V, a drain voltage  $V_{DL}$  relatively lower than the word line voltage  $V_{WL}$  such as 0.5V – 2V, a bit line voltage  $V_{BL}$  relatively lower the drain voltage  $V_{DL}$  such as 0V, and a deep P-well voltage relatively lower than the drain voltage such as 0V are provided.

[0055] In a light of foregoing, the non-volatile semiconductor memory cell having divided bit lines according to the present invention is characterized by use of a bit line selection device to control the main bit line and the sub bit line, such that the sub bit line and the main bit line in a designated sector have the same voltage to prevent the bit line from being overloaded.

[0056] Furthermore, formation of the bit line selection device and

memory cells on the different P-well and N-well effectively prevents the sectors from sharing the same N-well, resulting in significantly reduced disturbances when programming or erasing the bit line.

[0057] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the forgoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.